SEMICONDUCTOR PACKAGE INCLUDING LEADS WITH VERTICALLY DOWNSET INNER ENDS

ABSTRACT OF THE DISCLOSURE

[0053] A semiconductor package includes a chip mounting pad having a peripheral edge. The package further includes a semiconductor chip attached to the chip mounting pad. The package further includes a plurality of leads. Each lead includes an inner end and an opposing distal end. Each inner end is disposed adjacent the peripheral edge in spaced relation thereto and vertically downset with respect to each respective distal end. The package further includes at least one isolated ring structure disposed along the peripheral edge between the peripheral edge and the inner ends of the leads in spaced relation thereto. The ring structure is electrically connected to the semiconductor chip and an inner end of at least one of the leads.